WE CLAIM

1. Apparatus for processing data, said apparatus comprising:

at least one memory having a plurality of memory storage locations associated with respective memory addresses;

a self-test controller operable to control self-test of said at least one memory including generating physical memory address signals; and

a mapping circuit operable to map said physical memory address signals generated by said self-test controller to corresponding logical address signals for use by said at least one memory to perform a memory test based upon a physical position of memory storage locations.

2. Apparatus as claimed in claim 1, wherein said physical memory address signals include row address signals and column address signals for addressing a memory having a row and column layout.

3. Apparatus as claimed in claim 1, wherein said mapping circuit is operable to map first physical memory address signals addressing a first memory location and second physical memory address signals addressing a second memory location to first logical address signals addressing said first memory location and second logical address signals addressing said second memory location respectively such that a memory test being performed by said self-test controller and based upon relative physical position of said first memory location and said second memory location still operates when said at least one memory is addressed with said logical address signals.

4. Apparatus as claimed in claim 1, wherein said at least one memory is one of a synthesized memory and a custom memory.

5. Apparatus as claimed in claim 1, wherein said mapping circuit is part of an interface circuit disposed between said self-test controller and said at least one memory, said interface circuit serving to adapt values and timings of signals passed between said self-test controller and said at least one memory to accommodate differing value and timing properties of said at least one memory.

6. Apparatus as claimed in claim 1, further comprising a processor core, said processor core, said at least one memory and said self-test controller being formed together on an integrated circuit.

7. Apparatus as claimed in claim 1, comprising a plurality of memories, a mapping circuit being provided for each of said memories.

8. A method of testing a memory having a plurality of memory storage locations associated with respective memory addresses, said method comprising the steps of:

generating physical memory address signals; and

mapping said physical memory address signals to corresponding logical address signals for use by said at least one memory to perform a memory test based upon a physical position of memory storage locations.

9. A method as claimed in claim 8, wherein said physical memory address signals include row address signals and column address signals for addressing a memory having a row and column layout.

10. A method as claimed in claim 8, wherein first physical memory address signals addressing a first memory location and second physical memory address signals addressing a second memory location are mapped to first logical address signals addressing said first memory location and second logical address signals addressing said second memory location respectively such that a memory test being performed based upon relative physical position of said first memory location and said second memory location still operates when said at least one memory is addressed with said logical address signals.

11. A method as claimed in claim 8, wherein said at least one memory is one of a synthesized memory and a custom memory.

12. A method as claimed in claim 9, wherein values and timings of signals passed to said least one memory are adapted to accommodate differing value and timing properties of said at least one memory.

13. A method as claimed in claim 8, wherein a processor core and said at least one

memory are formed together on an integrated circuit.

14. A method as claimed in claim 8, comprising a plurality of memories, a mapping being performed for each of said memories being tested.